IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants:	Antonio Asaro et al.	Examiner:	Paul R. Myers
Serial No.:	10/074,064	Art Unit:	2111
Filing Date:	February 12, 2002	Docket No.:	00100.00.0130
Confirmation No.:	6702		

Title: **METHOD AND APPARATUS FOR A DATA BRIDGE IN A COMPUTER SYSTEM**

Mail Stop AF
Commissioner for Patents
P. O. Box 1450
Alexandria, VA 22313-1450

REMARKS FOR PRE-APPEAL BRIEF REQUEST FOR REVIEW

Dear Sir:

Applicants respectfully submit that the Examiner's rejections include clear errors because one or more claim limitations are not met by the cited references and the references do not teach what the Examiner alleges.

Claims 29-31 contain allowable subject matter and would be allowable if written in independent form to include the limitations of the base claim and any intervening claims. Remaining claims 1-28 and 33-35 stand rejected. Claims 1, 4-11, 13, 15-17, 19, 22-23, 25-28 and 34-35 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Gillespie et al. (U.S. Patent No. 5,859,987) in view of Suruguechi et al. (U.S. Patent No. 6,094,699) and Venkat (U.S. Patent No. 5,857,083).

As to claims 28, 34, and 35, the claims require, among other things, configuring registers, as opposed to writing data values to the registers. By way of example, the claimed registers are general purpose registers that are configured so that generic register definitions are defined by ROM contents. Mask values are loaded into register configuration circuits to then form registers as being readable and/or writable. By way of example, claims 28 and 34 include a configurable register that includes configured register logic and at least one register flop and at least one

masked value that generates a masked bit for the configuration logic. The configuration logic configures at least one register flop to be read and/or writable based on the at least one masked value. The claims are directed to configuring a register, as opposed to populating a register with data as alleged in the Office Action. The Office Action states that "this claim language makes clear that the mask value is used to screen out or let through (i.e., read and/or write) certain bits in the data value." (Response to Arguments section, page 2.) However, this is not what the claim language states. The claim language is not directed to screening out or letting through data bits in a data value, which is a different operation, namely, a post-configuration operation and the screening or letting through of data bits in a register. In contrast, Applicants are claiming the configuration operation as to whether a register is configured as a read or writable register, not a post-configuration data population operation, and instead claim using mask values in the configuration of the registers to be readable or writable.

Also by way of example, the claim language itself requires that the method (for example, see claim 35) requires conforming configurable registers by forming at least one register flop of the configurable registers to be readable and/or writable based on as least one mask value. Again, this operation "forms" or "configures" a register flop to be readable or writable independent of any data values stored therein. The interpretation and rejection dealing with claim language not present in Applicants' claim is believed to be improper. Screening out or letting through certain bits in a data value as alleged in the Office Action, as noted above, requires that the register already be configured as a writable or readable register – otherwise no data value in the register could be written or screened therefore. The cited references merely allow access to data values or bits in the register but are not used to configure the register to be readable or writable. Therefore, Applicants respectfully request withdrawal of the rejection.

Also, with regard to claim 1, the Examiner admits that Gillespie fails to show, teach, or suggest the data bridge having a read only memory for storing at least initial values and mask values for each ASIC of the plurality of ASICs.

The Examiner suggests that it would be obvious to one of ordinary skill in the art to combine the teachings of Gillespie and Suruguchi et al. to render the data bridge having a read only memory for storing mask values for each ASIC of the plurality of ASICs in order to consolidate configuration. However, Suruguchi et al. explicitly teach that the BASS control logic unit updates the registers in the second configuration register space (which includes the BASS 1 memory mask) with the values in the first configuration space when the values in the first configuration space are set and/or modified. (See column 8, lines 47-51.) Therefore, Suruguchi et al. explicitly teach away from using a read only memory for storing mask values because the BASS control logic would not be able to update a read only memory. Accordingly, it would not be obvious for one skilled in the art to combine the teachings of Gillespie and Suruguchi et al. to render the data bridge having a read only memory for storing mask values for each ASIC of the plurality of ASICs in order to consolidate configuration.

Venkat fails to cure the deficient teachings of Gillespie and Suruguchi et al. As best understood by Applicants, Venkat discloses a bus interface device for interfacing a secondary peripheral bus with a system having a host CPU and a primary peripheral bus. The bus interface of Venkat enables "virtual integration" of multiple physically distinct peripheral devices so that the collection of devices can function as a single integrated unit. The "virtually integrated" devices can share resources such as a dedicated bus, memory space, and memory bandwidth just as if the devices were physically integrated. An intelligent device configuration process and a dynamic internal memory map allow each peripheral device to be independently added to the

system, removed from the system, or upgraded just as if each device was a completely separate peripheral. The bus interface provides a dedicated secondary bus that enables multimedia and graphics bus traffic to be isolated from the CPU's primary peripheral bus. Applicants can find no mention of data bridge having a read only memory for storing mask values for each ASIC of the plurality of ASICs. Therefore, reconsideration and withdrawal of the rejection of claim 1 is respectfully requested.

As noted above, there is no teaching, suggestion or motivation to combine the references (and there is actually a teaching away), nor is there evidence of any external market forces that provide motivation to combine the references. For argument sake even if the teachings of the references were somehow combinable, their combination is still void of the claimed subject matter since the references alone or in combination are totally missing any teaching of a mask bit based register read/write configuration scheme.

Claim 10 is allowable for at least similar reasons as claim 1. For example, the references do not teach or suggest forming configurable registers as claimed. Therefore, reconsideration and withdrawal of the rejection of claim 10 is respectfully requested.

Claims 2-9, 11-18, and 34-35 each ultimately depend on claims 1 and 10 and are allowable for at least similar reasons. Claims 2-9, 11-18, and 34-35 are also believed to be allowable for having novel and non-obvious subject matter. Therefore, reconsideration and withdrawal of the rejection of claims 2-9, 11-18, and 34-35 is respectfully requested.

Claim 35 is allowable for at least similar reasons as claim 28. Therefore, reconsideration and withdrawal of the rejections of claim 35 is respectfully requested.

Reconsideration and withdrawal of the rejection of the claims is respectfully requested and a Notice of Allowance is respectfully requested.

Respectfully submitted,

Date: 5-16-12

By: _____
Christopher J. Reckamp
Registration No. 34,414

Vedder, Price, Kaufman & Kammholz, P.C.
222 N. LaSalle St., Suite 2600
Chicago, Illinois 60601
phone: (312) 609-7599
fax: (312) 609-5005